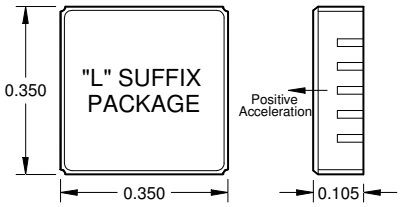
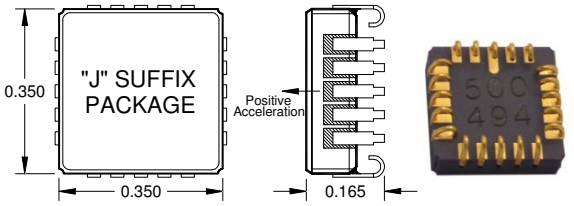
MODEL 1410
DIGITAL SURFACE MOUNT ACCELEROMETER

- **Digital Pulse Density Output**
- Drop-In Replacement for Model 1010
- Integrated Sensor & Amplifier
- -55 to +125 °C Operation
- +5 VDC, 2 mA Power (typical)
- LCC or J-Lead Surface Mount Package
- Responds to DC & AC Acceleration
- No External Reference Voltage
- Easy Interface to Microprocessors, TTL/CMOS Compatible
- Nitrogen Damped & Hermetically Sealed
- Capacitive Micromachined & Serialized for Traceability
- Good EMI Resistance

AVAILABLE G-RANGES

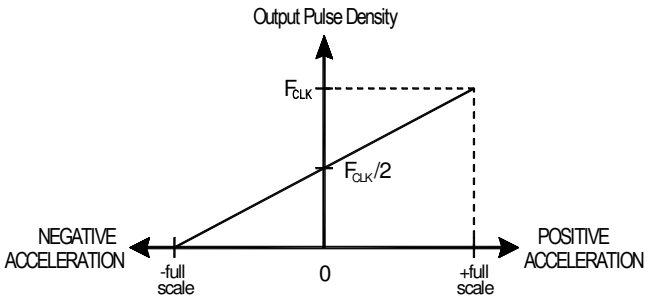
FULL SCALE ACCELERATION	20 PIN JLCC	20 PIN LCC
± 2 g	1410J-002	1410L-002
± 5 g	1410J-005	1410L-005
± 10 g	1410J-010	1410L-010
± 25 g	1410J-025	1410L-025
± 50 g	1410J-050	1410L-050
± 100 g	1410J-100	1410L-100
± 200 g	1410J-200	1410L-200





DESCRIPTION

The Model 1410 is an integrated accelerometer for use in zero to medium frequency instrumentation applications. Each miniature, hermetically sealed package combines a micro-machined capacitive sense element and a custom integrated circuit that includes a sense amplifier and sigma-delta A/D converter. It is relatively insensitive to temperature changes and gradients. Each device is marked with a serial number on its top and bottom surfaces for traceability. An optional calibration test sheet (1410-TST) is also available which lists the measured bias, scale factor, linearity, operating current and frequency response.



ZERO (DC) TO MEDIUM FREQUENCY APPLICATIONS

ROBOTICS · TILT · VIBRATION · AUTOMOTIVE · IMPACT · INSTRUMENTATION · MONITOR · OEM

PERFORMANCE

INPUT RANGE	FREQUENCY RESPONSE (MIN, 3 DB)	SENSITIVITY, DIFFERENTIAL	MAX. MECHANICAL SHOCK (0.1 MS)
g	Hz	kHz/g	g (peak)
±2	0 – 400	62.5	2000
±5	0 – 500	25	
±10	0 – 700	12.5	5000
±25	0 – 1000	5	
±50	0 – 1300	2.5	
±100	0 – 1600	1.25	
±200	0 – 1900	0.625	

By Model: $V_{DD}=V_R=5.0$ VDC, $F_{CLK}=250$kHz, $T_C=25°C$ **Note 1**: Sensitivity typical at clock frequency 250kHz

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

PERFORMANCE - ALL VERSIONS

All Models: Unless otherwise specified V_{DD}=V_R=5.0 VDC, F_{CLK}=250 kHz, T_C=25°C

PARAMETER	MIN	TYP	MAX	UNITS
Cross Axis Sensitivity		2	3	± %
Bias Calibration Error [1]		0.2	0.5	± % of F_{CLK} (span)
Bias Temperature Shift (T_C= -55 to +125°C) [1]	-200	0	+200	(PPM of F_{CLK})/°C
Scale Factor Calibration Error [1,2]		0.75	2	± %
Scale Factor Temperature Shift (T_C= -55 to +125°C) [1]	0		+200	PPM/°C
Non-Linearity (-90 to +90% of Full Scale) [1,2]		0.5	1.0	± % of span
Long Term Bias Stability		1000	2000	± PPM of span
In Run Bias Stability		18	30	± PPM of span
Long Term Scale Factor Stability		500	1000	± PPM
Turn-On Transient (in less than 0.5ms)		38		± PPM of span
Operating Voltage (V_{DD} vs. GND)	4.5	5.0	5.5	Volts
Operating Current (I_{DD} + I_{VR})[1]		2	3	mA
Clock Input Voltage Range (with respect to GND)	-0.5		V_{DD}+0.5	Volts
Mass 'L' Package (add 0.06 grams for 'J' package)		0.62		Grams

Note 1: Tighter tolerances may be available on special order. Note 2: 100g and greater versions are tested and specified from -65 to +65g

DC CHARACTERISTICS

V_{DD}=V_R=5.0 VDC, T_C= 55 to +125°C

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{T-}	Negative Going Threshold Voltage (CLK)	0.9	1.7		V	
V_{T+}	Positive Going Threshold Voltage (CLK)		3.0	3.7	V	
V_H	Hysteresis Voltage (CLK)	0.5	1.3		V	
V_{OL}	Output Low Voltage (CNT, DIR, CLK/2)			0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage (CNT, DIR, CLK/2)	V_{DD} - 0.4			V	I_{OH} = 2.0 mA
I_I	Input Leakage Current (CLK)			10	µA	V_I = 0 to V_{DD}
C_{IO}	Pin Capacitance			10	pF	1 MHz, T_A = 25°C
I_{DD}+I_{VR}	Operating Current		2	3	mA	F_{CLK} = 250kHz

DC CHARACTERISTICS

V_{DD}=V_R=5.0 VDC, T_C= -55 to +125°C, Load Capacitance=50pF.

PARAMETER	MIN	TYP	MAX	UNITS
CLK input frequency	100	250	1000	kHz
CLK input rise/fall time			50	ns
CLK duty cycle	45	50	55	%
CLK fall to DIR fall	40	85	195	ns
CLK fall to DIR rise	40	90	205	ns
CLK rise to valid CNT out	40	90	230	ns
CLK fall to CNT fall	40	85	205	ns
CLK fall to CLK/2 rise/fall	40	90	210	ns

MAXIMUM RATINGS*

Case Operating Temperature [4]	-55 to +125°C
Storage Temperature [4]	-55 to +125°C
Voltage on V_{DD} to GND	-0.5V to 6.5V
Voltage on Any Pin (except DV) to GND [3]	-0.5V to V_{DD}+0.5V
Voltage on DV to GND [5]	±15V
Power Dissipation	20 mW

**** NOTICE:*** *Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at or above these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and lifespan.*

Note 3: Voltages on pins other than DV, GND or V_{DD} may exceed 0.5 volt above or below the supply voltages provided the current is limited to 1 mA.

Note 4: Operation may continue with limited exposure up to 175°C. Minimal exposure over 125°C recommended for maximum lifespan.

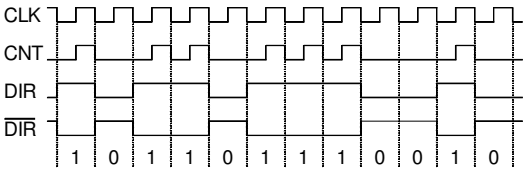
Note 5: The application of DV voltages higher than required to bring the output to positive full scale may cause device damage.

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

OPERATION

The Model 1410 produces a digital pulse train in which the density of pulses (number of pulses per second) is proportional to applied acceleration. It requires a single +5 volt power supply and a TTL/CMOS level clock of 100kHz-1MHz. The output is ratiometric to the clock frequency and independent of the power supply voltage. Two forms of digital signals are provided for direct interfacing to a microprocessor or counter. The sensitive axis is perpendicular to the bottom of the package, with positive acceleration defined as a force pushing on the bottom of the package. External digital line drivers can be used to drive long cables or when used in an electrically noisy environment.

SIGNAL DESCRIPTIONS

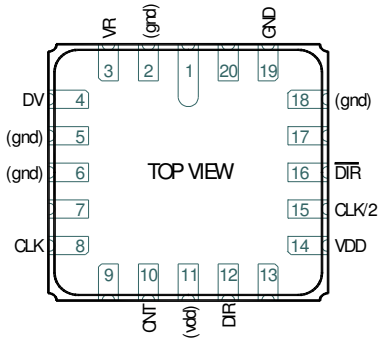


VDD and GND (power): Pin 14 (VDD) & pin 19 (GND). Additionally, tie pins 3 & 11 to VDD & pins 2, 5, 6 & 18 to GND.

CLK (input): Pin 8. Reference clock input. This hysteresis threshold input must be driven by a 50% duty cycle square wave signal. Factory Calibration is performed at 250 kHz, which is the recommended clock frequency for best results. Operation at frequencies as low as 100 kHz or as high as 1 MHz are possible, however a slight bias shift may result.

CNT (output): Pin 10. Count output. A return-to-zero type digital pulse stream whose pulse width is equal to the input CLK logic high time. The CNT pulse rate increases with positive acceleration. The device experiences positive (+1g) acceleration with its lid facing up in the earth's gravitational field. This signal is meant to drive an up-counter directly.

DIR and $\overline{\text{DIR}}$ (output): Pins 12 & 16 respectively. Direction output. This output is updated at the fall of each clock cycle. It is high during clock cycles when a high going CNT pulse is present and low during cycles when no CNT pulse is present. A non- return-to-zero signal meant to control the count direction (i.e. up or down) of a counter. **DIR** can be low pass filtered to produce an analog measure of the acceleration. $\overline{\text{DIR}}$ is the complement of DIR and is provided for use in driving differential transmission lines.



PINOUT (LCC & JLCC)

DV (input): Pin 4. Deflection Voltage. Normally left open. A test input that applies an electrostatic force to the sense element, simulating a positive acceleration. The nominal voltage at this pin is ⅓V_{DD}. DV voltages higher than required to bring the output to positive full scale may cause device damage.

VR (input): Pin 3. Voltage Reference. Tie directly to V_{DD} (+5V). A 0.1µF bypass capacitor is recommended at this pin.

CLK/2 (output): Pin 15. Clock divided by 2. A buffered clock output whose frequency equals CLK divided by 2.

**** Pins 1, 7, 9, 13, 17, and 20 are reserved for future use and should remain unused ****

USING THE COUNT (CNT) OUTPUT: Pulses from the CNT output are meant to be accumulated in a hardware counter. Each pulse accumulation or sample, reflects the average acceleration (change in velocity) over that interval. The sample period or "gate time" over which these pulses are accumulated determines both the bandwidth and quantization of the measurement.

$$\text{Quantization (g's)} = \frac{g_{SPAN} \cdot f_{SR}}{f_{CLK}}$$

$$f_{CNT} = f_{CLK} \left(\frac{1}{2} + \frac{g_{FORCE}}{g_{SPAN}} \right)$$

$$g_{FORCE} = g_{SPAN} \left(\frac{f_{CNT}}{f_{CLK}} - \frac{1}{2} \right)$$

Where:

g_{SPAN} = 2* (full scale acceleration in g's)

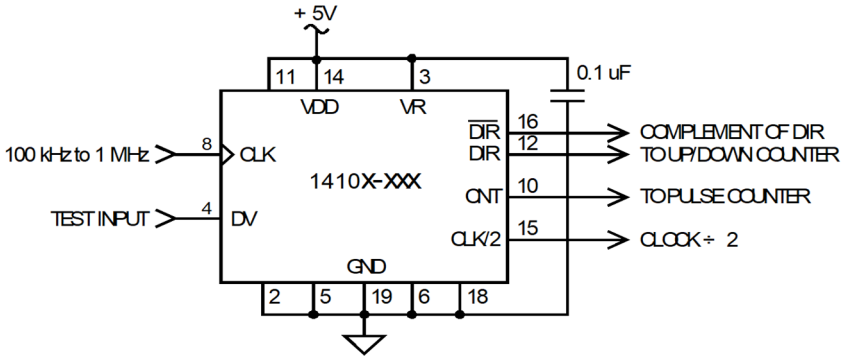
f_{SR} = CNT sample rate in Hertz

f_{CLK} = accelerometer clock rate in Hertz

f_{CNT} = CNT pulse rate in pulses/sec

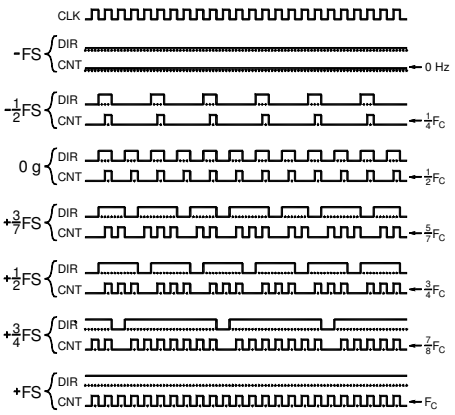
g_{FORCE} = acceleration in gravity units

1 g* = 9.807 m/s^2 or 32.18 ft/s^2 * reflects location of SDI facility



RECOMMENDED CONNECTIONS

The first equation above shows that as the sample rate is reduced (i.e. a longer sample period), the quantization becomes finer but bandwidth is reduced. Conversely, as the sample rate is increased, quantization becomes coarser but the bandwidth of the measurement is increased. The second and third equations show how the CNT pulse frequency equates to the applied g-force. When using a frequency counter to monitor the CNT output pulse rate, a counter with a DC coupled input must be used. The CNT output is a return-to-zero signal whose duty cycle varies from zero to fifty percent, from minus full scale to positive full-scale acceleration. A frequency counter with an AC coupled input will provide an erroneous reading as the duty cycle varies appreciably from fifty percent. The figure to the left illustrates how the CNT and DIR outputs vary as the accelerometer is subjected to accelerations from minus full scale (-FS) to plus full scale (+FS).



DEFLECTION VOLTAGE (DV) TEST INPUT: This test input applies an electrostatic force to the sense element, simulating a positive acceleration. It has a nominal input impedance of 32 kΩ and a nominal open circuit voltage of ⅓V_{DD}. For best accuracy during normal operation, this input should be left unconnected or connected to a voltage source equal to ⅓ of the V_{DD} supply.

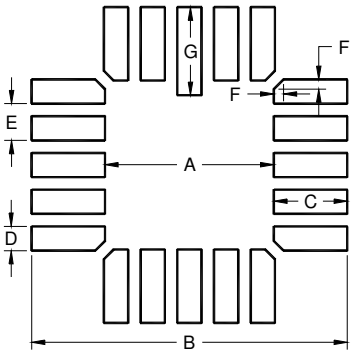
$$\Delta f \approx k(V_{DV} - \frac{1}{3} V_{DD})^2$$

The change in output pulse rate (Δf) is proportional to the square of the difference between the voltage applied to the DV input (V_{DV}) and ⅓V_{DD}. Only positive shifts in the output pulse rate may be generated by applying voltage to the DV input. When voltage is applied to the DV input, it should be applied gradually. The application of DV voltages greater than required to bring the output to positive full scale may cause device damage. The proportionality constant (k) varies for each device and is not characterized.

ESD and LATCH-UP CONSIDERATIONS: The model 1410 accelerometer is a CMOS device subject to damage from large electrostatic discharges. Diode protection is provided on the inputs and outputs but care should be exercised during handling to assure that the device is placed only on a grounded conductive surface. Individuals and tools should be grounded before coming in contact with the device. Do not insert the model 1410 into (or remove it from) a powered socket.

RECOMMENDED CONNECTIONS

DIM	Inch	mm
A	.230	5.84
B	.430	10.92
C	.100	2.54
D	.033	0.84
E	.050	1.27
F	.013	0.33
G	.120	3.05



RoHS Compliance: The model 1410 does not contain elemental lead and is RoHS compliant.

Soldering: Solder reflow should not exceed 239°C, exceeding this temperature may result in permanent damage

Pre-Tinning of Accelerometer Leads is Recommended: To prevent gold migration embrittlement of the solder joints, it is best to pre-tin the accelerometer leads.

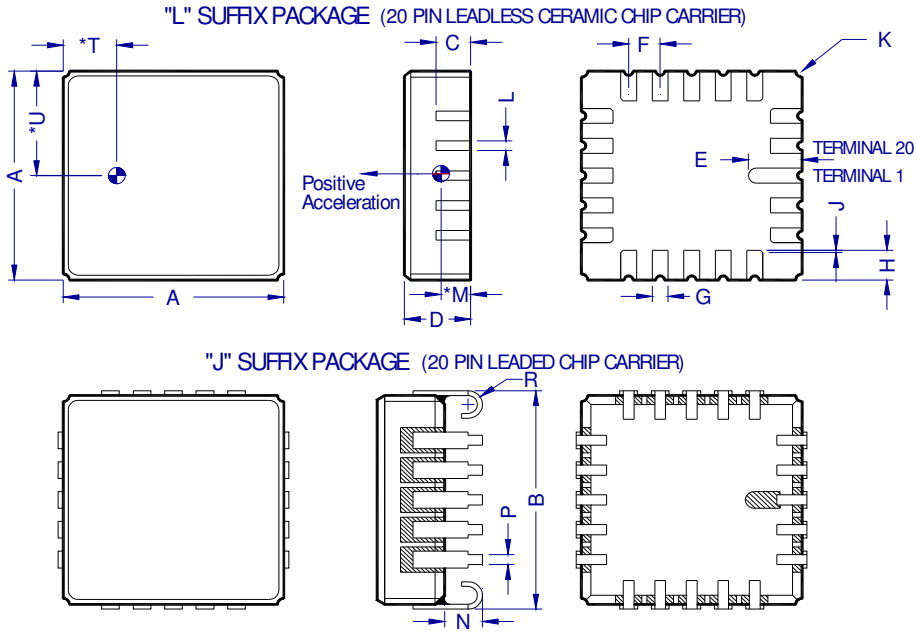
Solder Contact Plating Information: The plating composition and thickness for the solder pads and castellations on the "L" suffix (LCC) package are 60 to 225 micro-inches thick of gold (Au) over 80 to 350 micro-inches thick of nickel (Ni) over a minimum of 5 micro-inches thick of moly-manganese or tungsten refractory material. The J-Lead package top layer is 100 to 225 microinches thick of 99.7% gold (Au) over 80 to 350 microinches thick of electroplated nickel (Ni).

Recommended Solder Pad Pattern: The recommended solder pad size and shape for both the LCC and J LCC packages is shown in the diagram and table below. These dimensions are recommendations only and may or may not be optimum for your particular soldering process.

Do not use ultrasonic cleaners. Ultrasonic cleaning will void the warranty and may break internal wire bonds.

PACKAGE DIMENSIONS

1. *Dimensions “M,” “T,” and “U” locate sensing element’s center of mass.
2. Lid is electrically tied to terminal 19 (GND).
3. Controlling dimension: Inch.
4. Terminals are plated with 60 microinches min gold over 80 microinches min nickel. This plating specification does not apply to the Pin-1 identifier mark on the bottom of the J-lead package version.
5. Package: 90% min alumina (black), lid: solder sealed kovar.



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.342	0.358	8.69	9.09
B	0.346	0.378	8.79	9.60
C	0.055 TYP		1.40 TYP	
D	0.095	0.115	2.41	2.92
E	0.085 TYP		2.16 TYP	
F	0.050 BSC		1.27 BSC	
G	0.025 TYP		0.64 TYP	
H	0.050 TYP		1.27 TYP	
J	0.004 x 45°		0.10 x 45°	
K	0.010 R TYP		0.25 R TYP	
L	0.016 TYP		0.41 TYP	
* M	0.066 TYP		1.68 TYP	
N	0.050	0.070	1.27	1.78
P	0.017 TYP		0.43 TYP	
R	0.023 R TYP		0.58 R TYP	
* T	0.085 TYP		2.16 TYP	
* U	0.175 TYP		4.45 TYP	